PLL/DLL CIRCUITRY PROGRAMMABLE FOR
HIGH BANDWIDTH AND LOW BANDWIDTH APPLICATIONS

ABSTRACT OF THE DISCLOSURE

An integrated circuit including a phase lock loop or delay lock loop (PLL/DLL) circuit comprising: a clock input terminal for accepting a clock signal; a phase/frequency detector (PFD) circuit including a reference clock input connected to the clock input terminal and including a PFD feedback input and including a PFD output; a charge pump (CP) circuit; at least one external feedforward output terminal; a loop filter (LF); a loop controlled signal source (LCSS); and a feedback circuit connected between a LCSS output and the PFD feedback input, the feedback circuit including, an external feedback input terminal; first frequency selection circuitry to produce a first programmable feedback signal; second frequency selection circuitry to produce a second feedback signal ; and multiplex circuitry connected with the LCSS output, the external feedback input terminal and the first and second frequency selection circuitry, to cause either the first programmable feedback signal or the second programmable feedback signal to be coupled to the PFD feedback input.